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(54) ORGANIC ELECTROLUMINESCENCE DISPLAY PANEL

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(52) **U.S. Cl.** **257/211**

(57) **ABSTRACT**

According to an aspect of the present invention, an organic electro-luminescence display panel is provided, which includes: an insulating substrate; a polysilicon layer formed on the substrate; a first insulating layer formed on the polysilicon layer; a gate wire formed on the first insulating layer; a second insulating layer formed on the gate wire; a data wire formed on the second insulating layer and including first and second portions; a pixel electrode connected to the first portion of the data wire; a partition defining an area on the pixel electrode; an organic light emitting member formed in the area on the pixel electrode; a common electrode formed on the light emitting member; and a planar supply voltage electrode disposed between the pixel electrode and the substrate and connected to the second portion of the data wire.

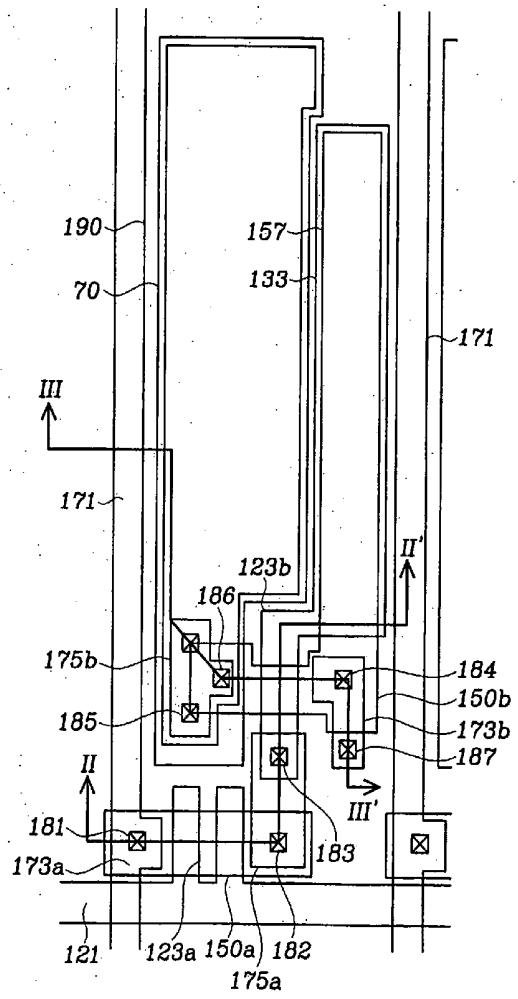

FIG.1

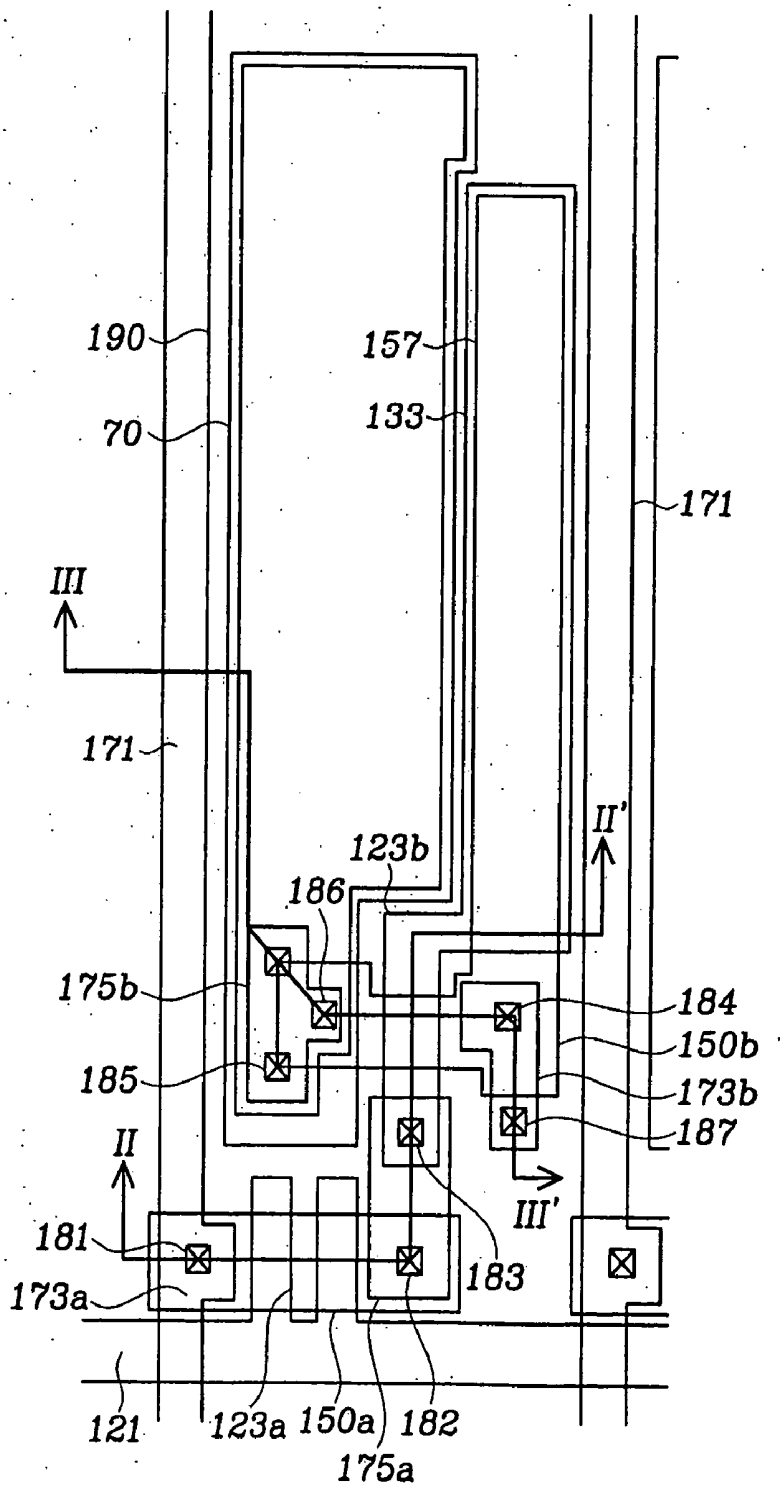
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FIG.2

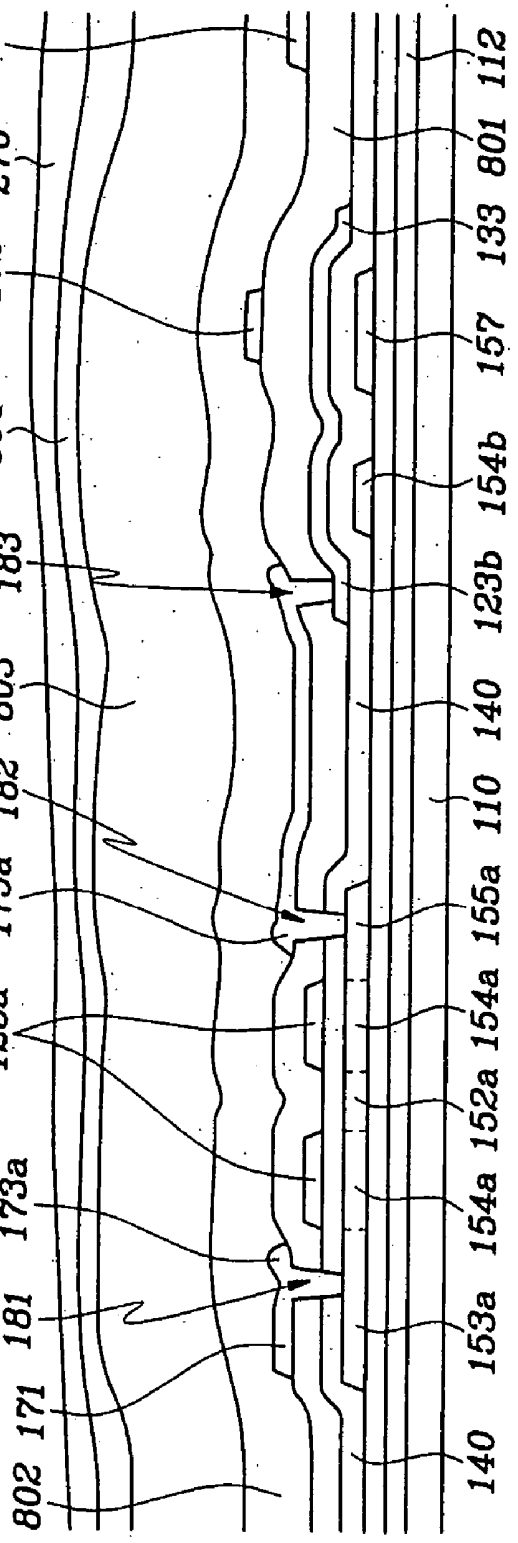
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FIG. 3

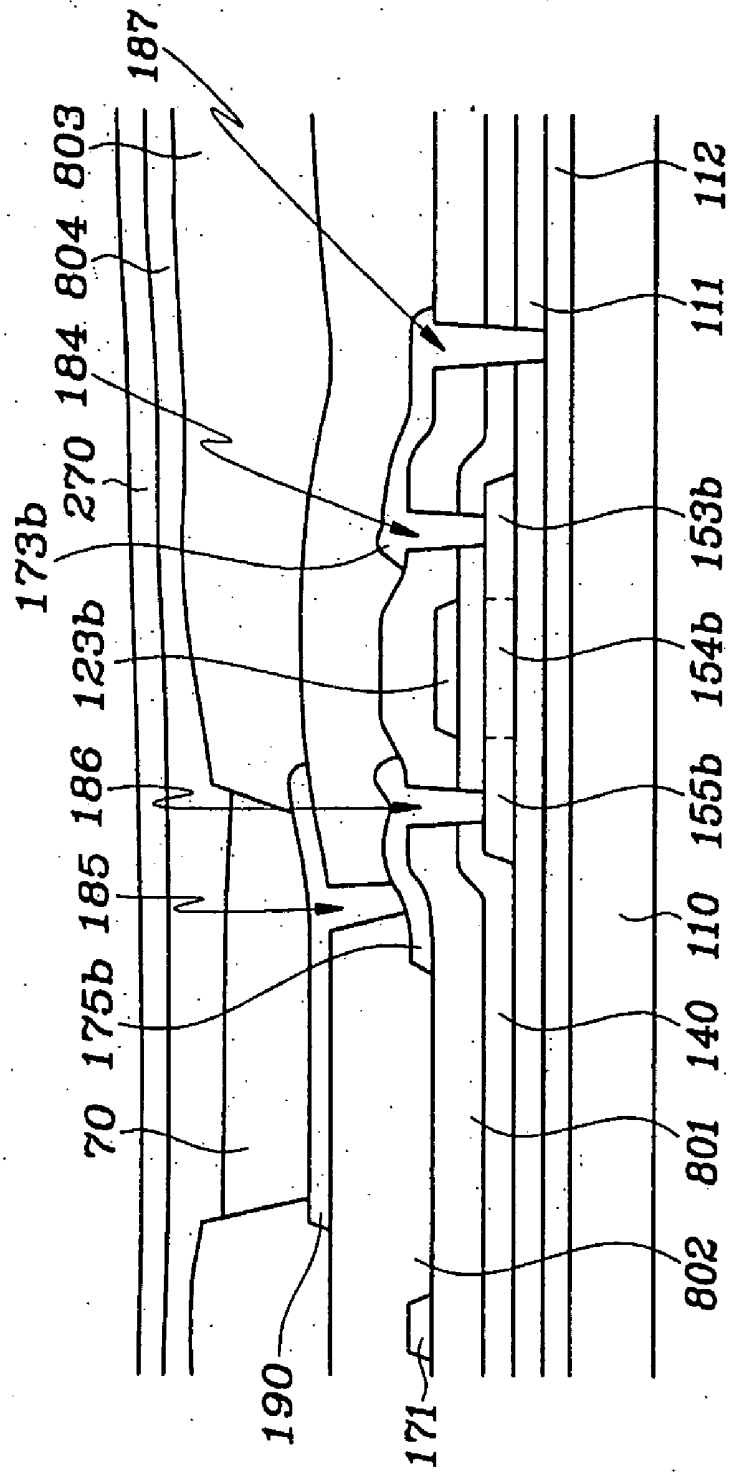
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FIG. 4A

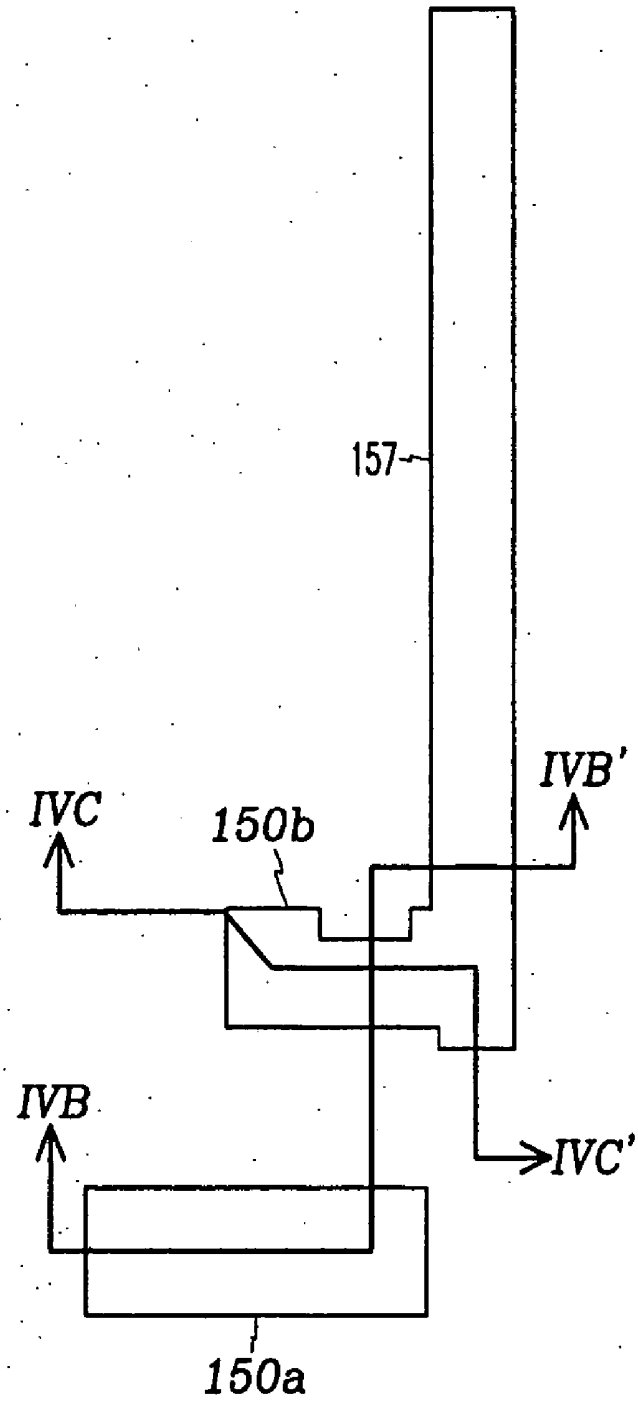


FIG.4B

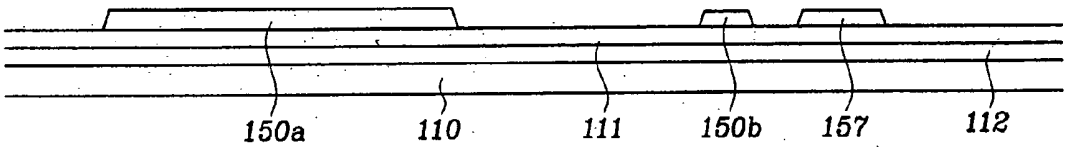


FIG.4C

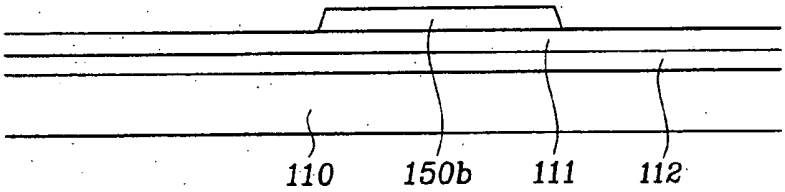


FIG.5A

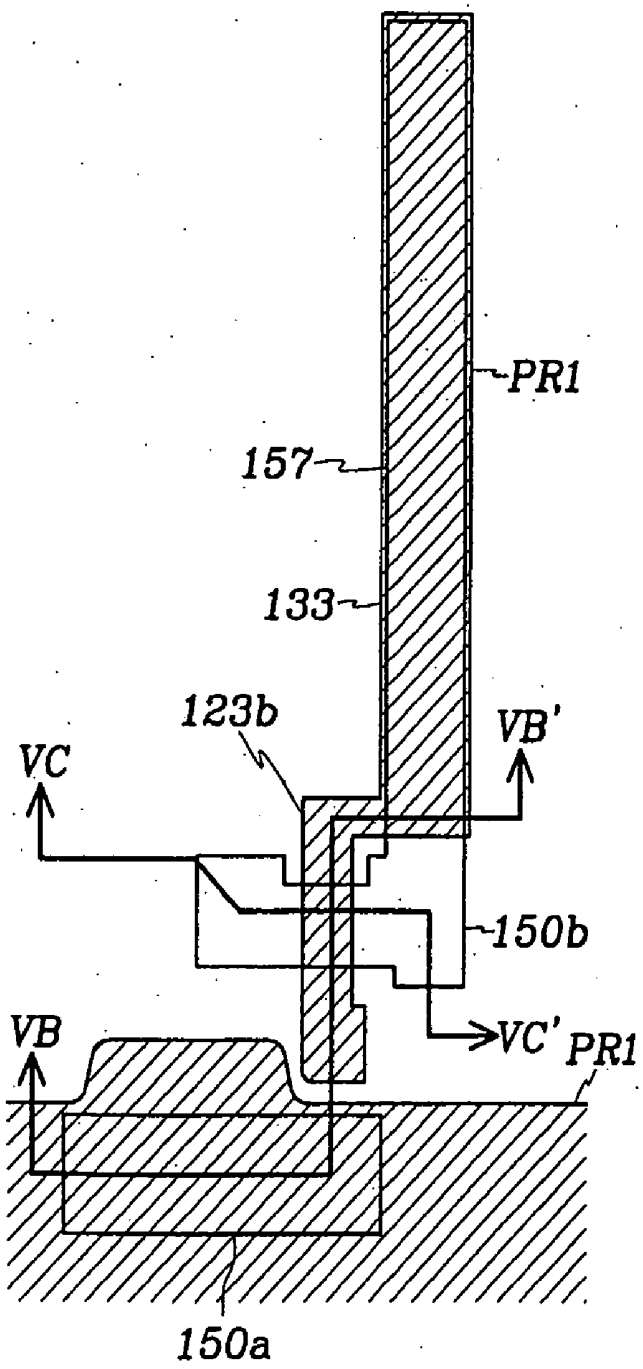
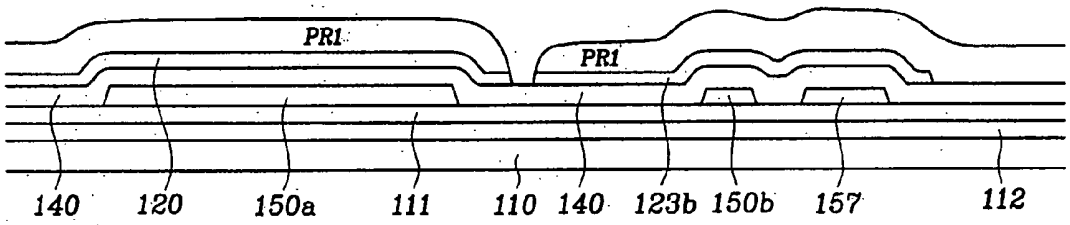


FIG.5B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123b
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157
112

FIG.5C

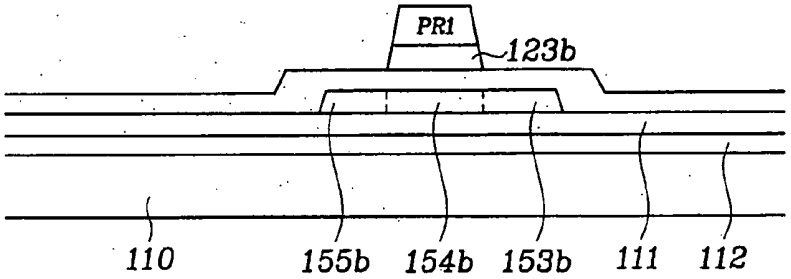
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FIG.6A

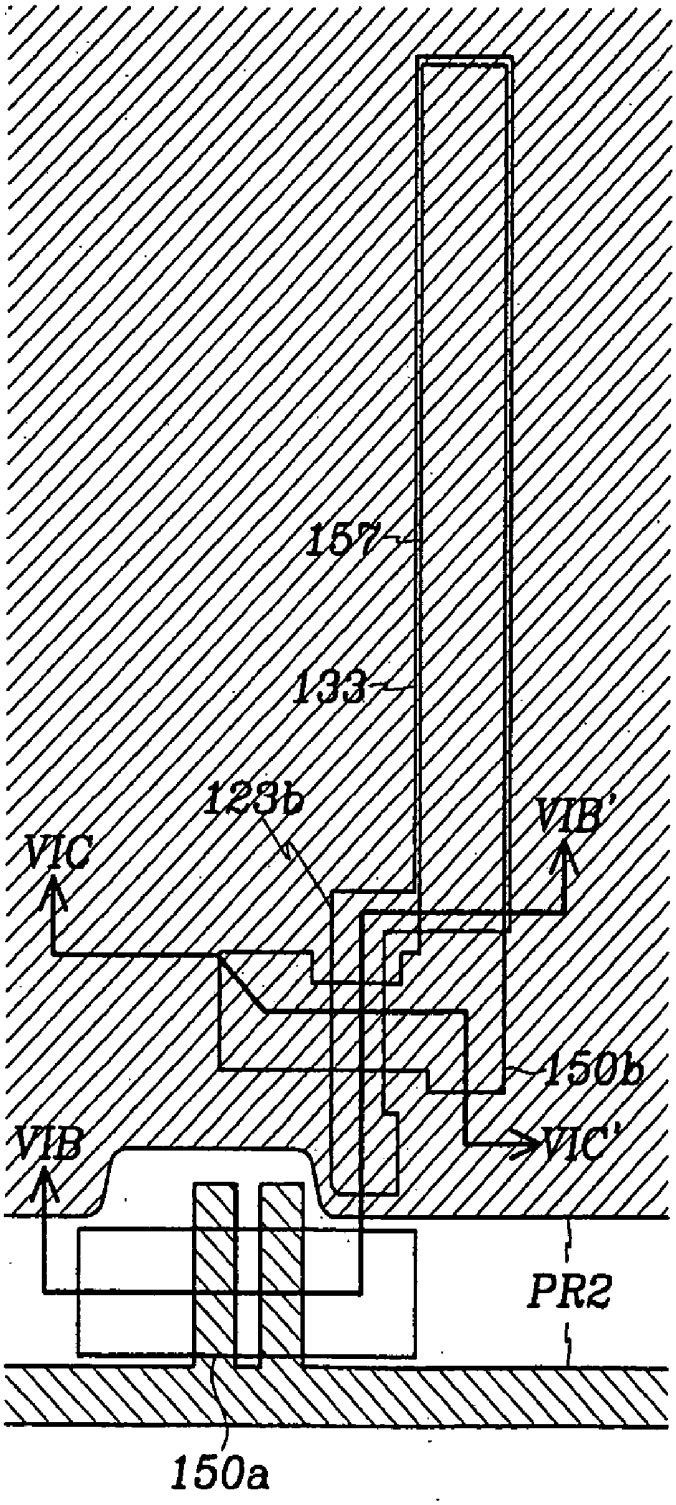
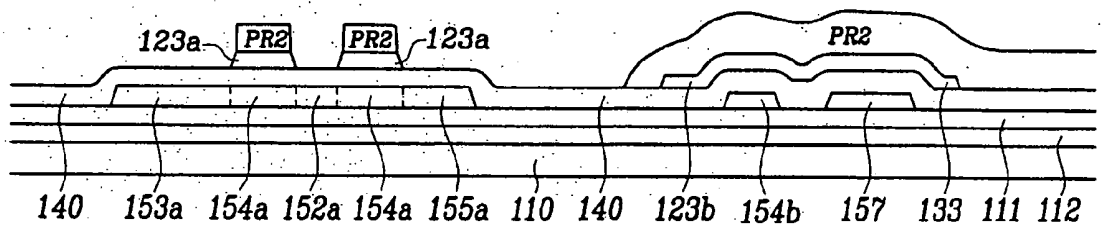


FIG.6B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PR2
123a
PR2
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140
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154b
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133
111
112

FIG.6C

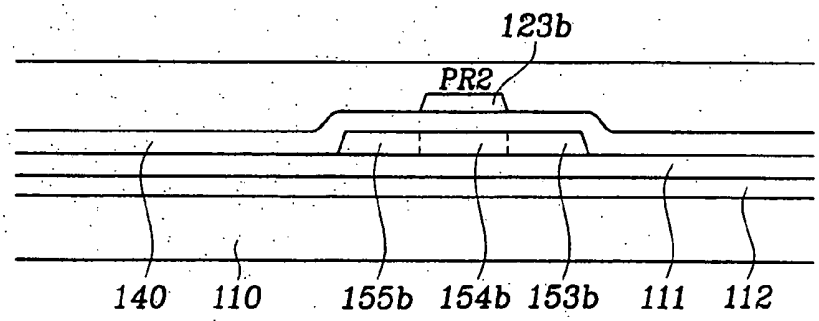
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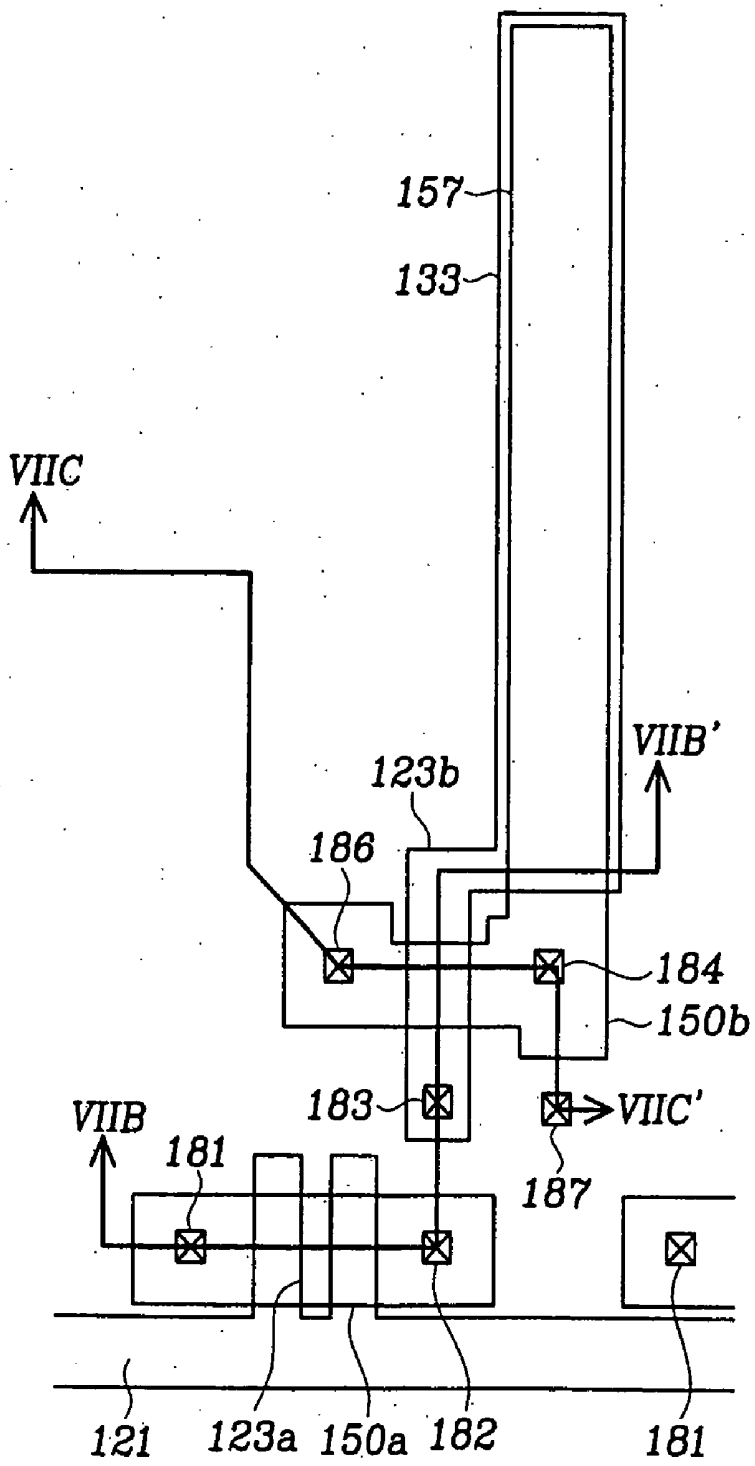
FIG. 7A


157
133
VIIC
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123b
186
184
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VIIB
181
187
121
123a
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182
181

FIG. 7B

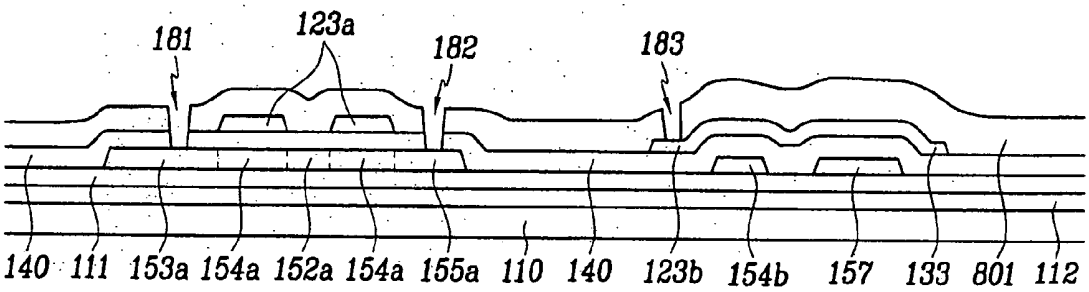
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FIG. 7C

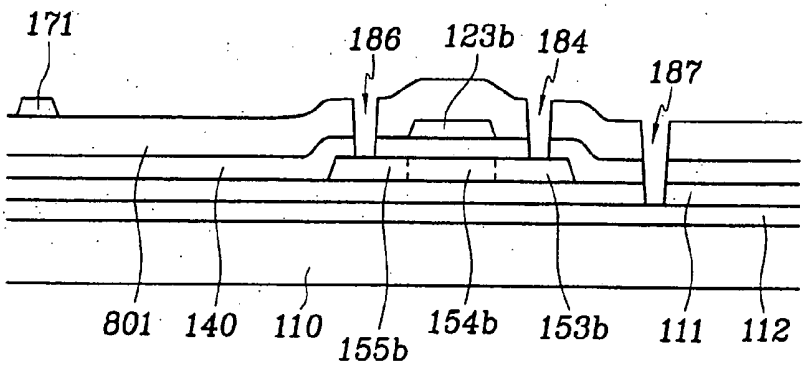
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FIG. 8A

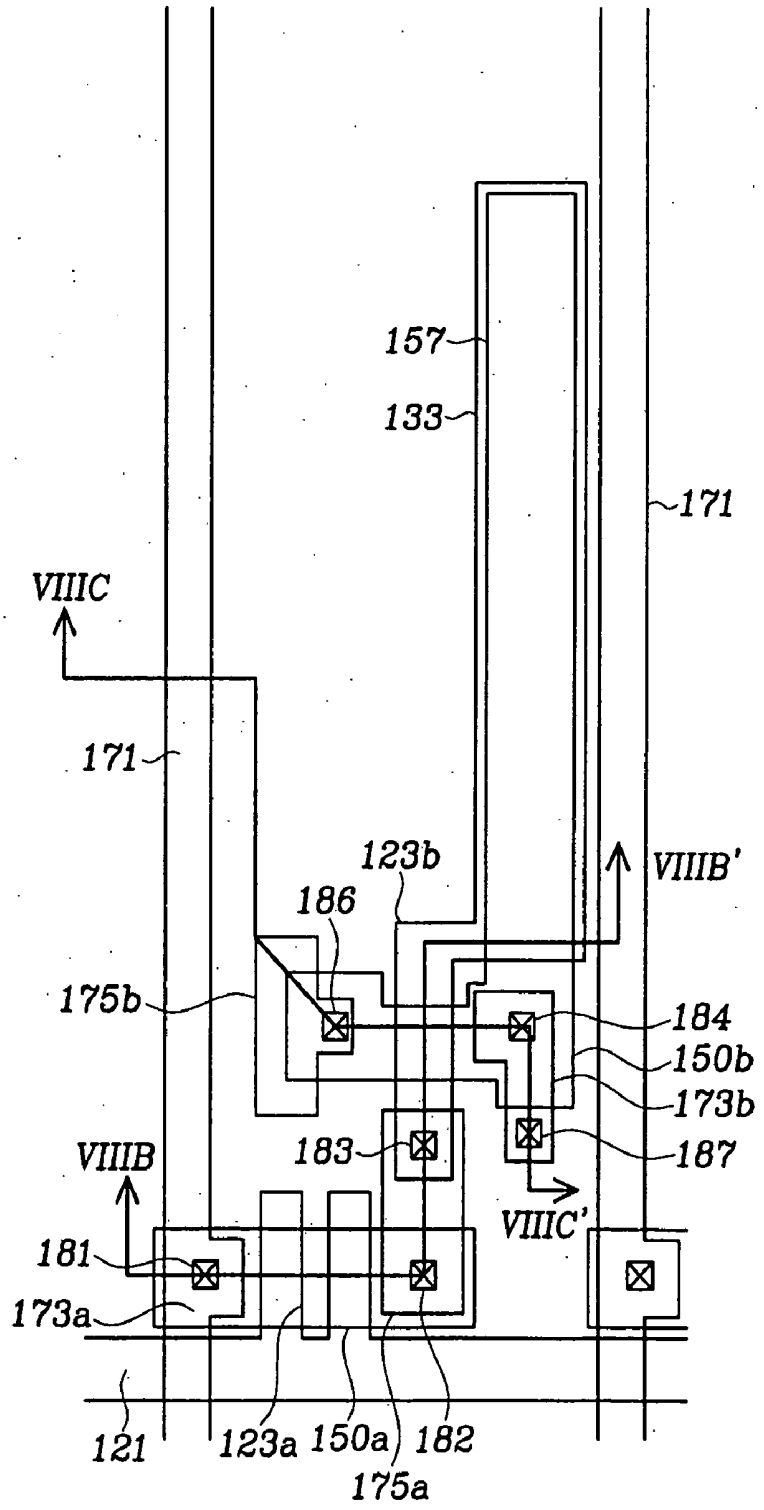
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FIG.8B

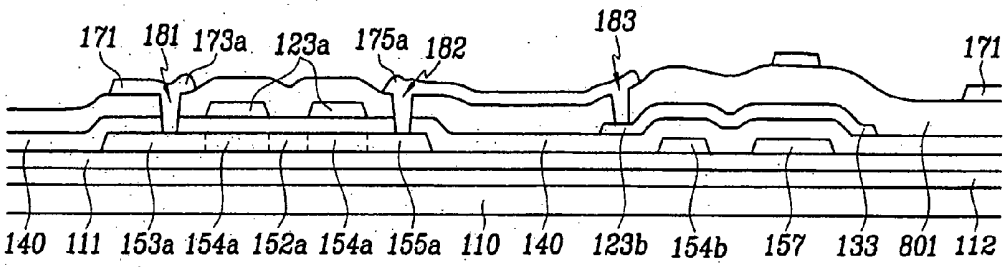
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FIG.8C

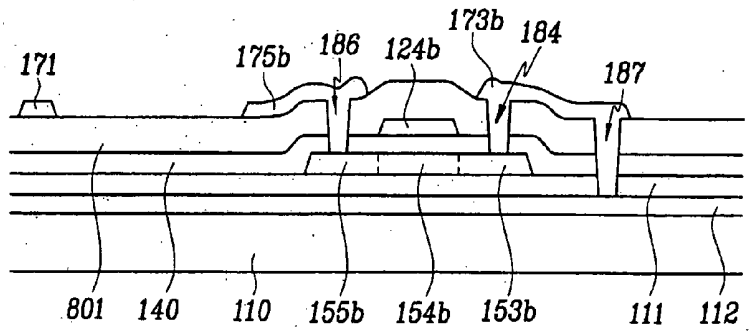
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FIG. 9A

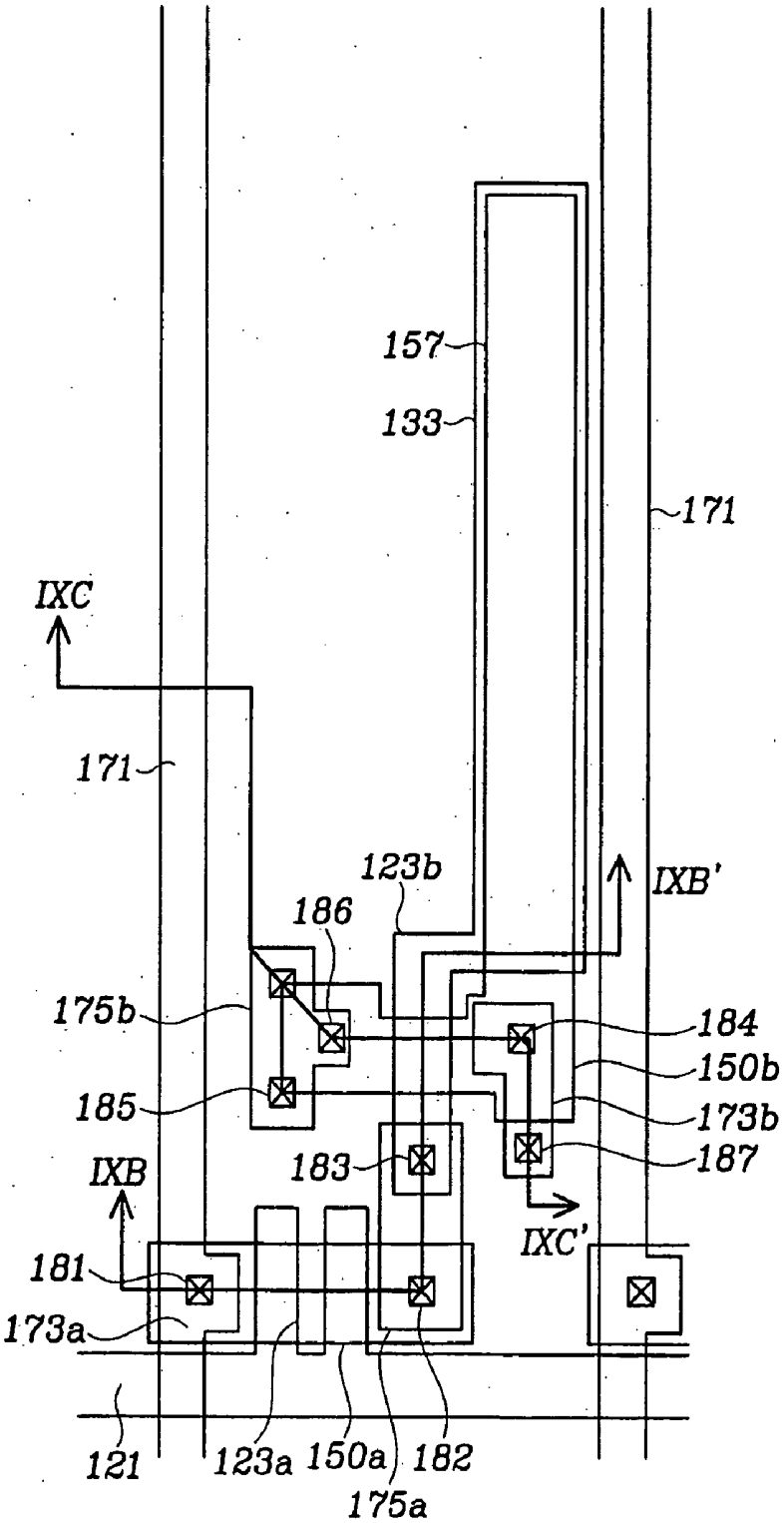
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FIG.9B

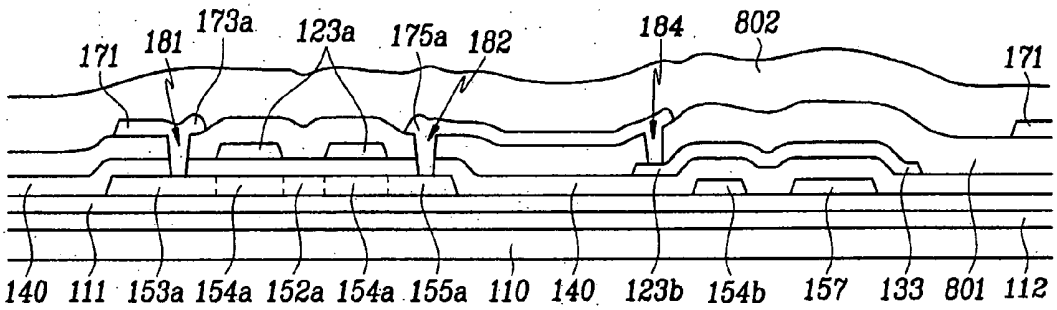
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FIG.9C

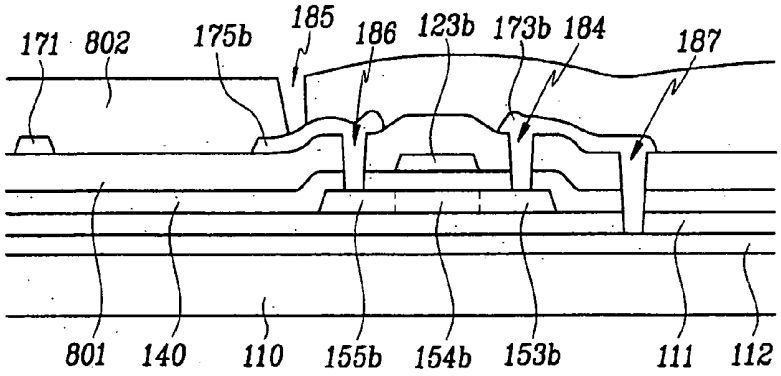
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FIG.10A

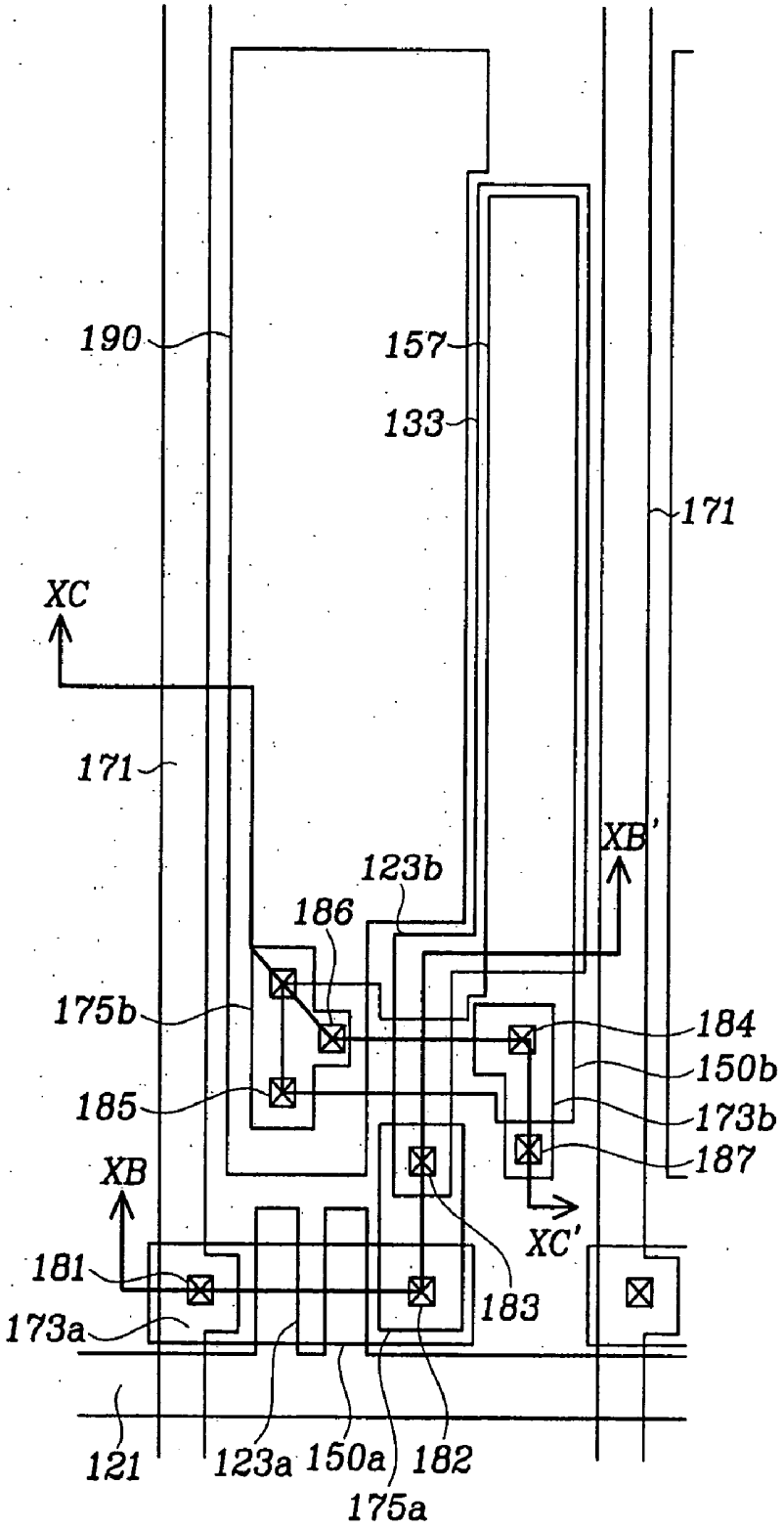
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FIG.10B

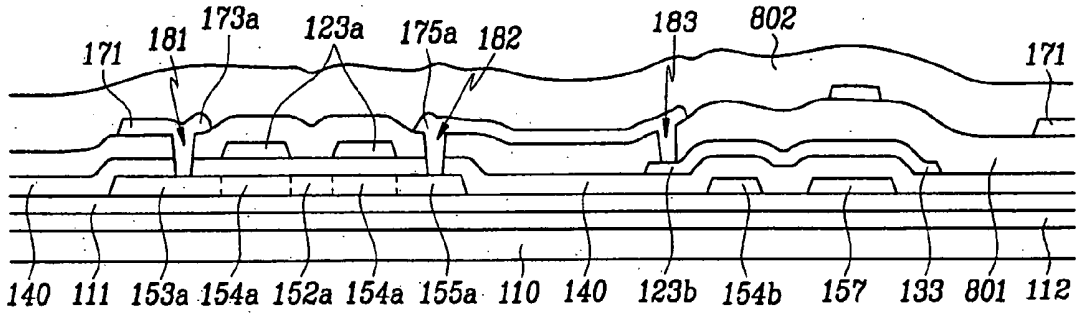

FIG.10C

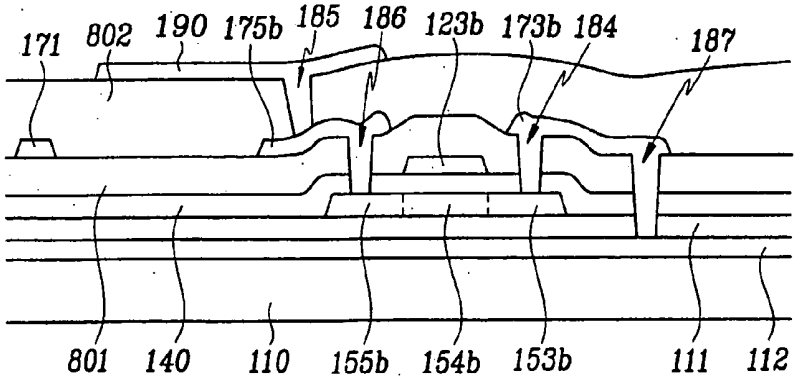

FIG.11

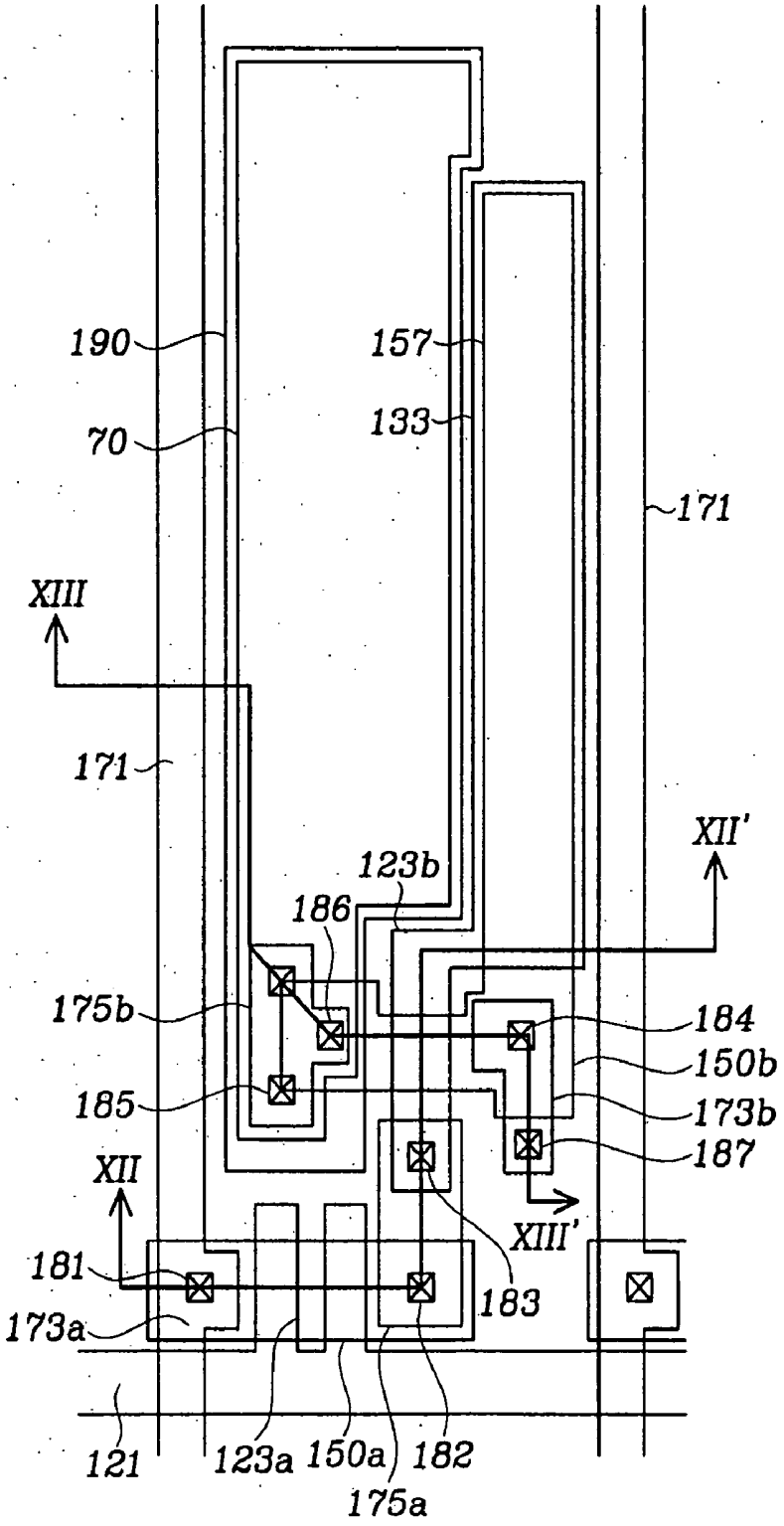
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FIG.12

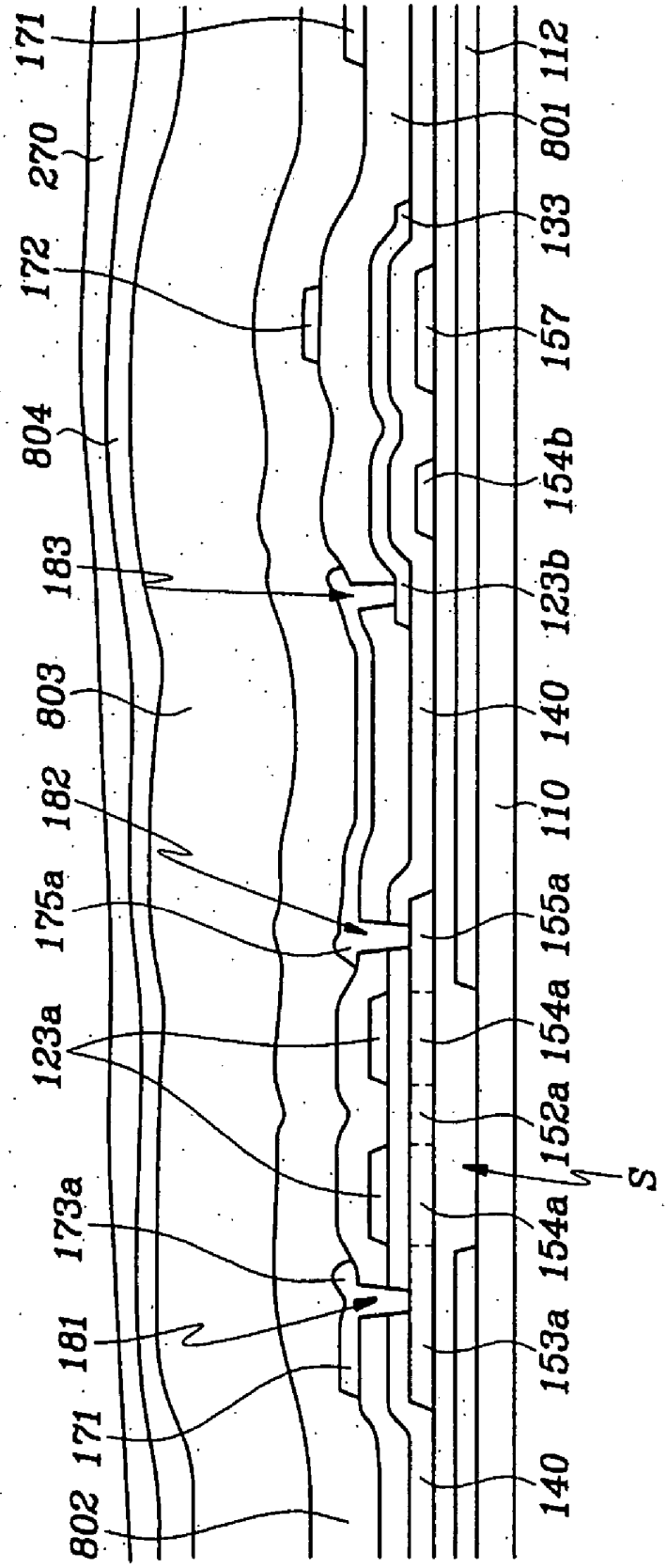
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FIG.13

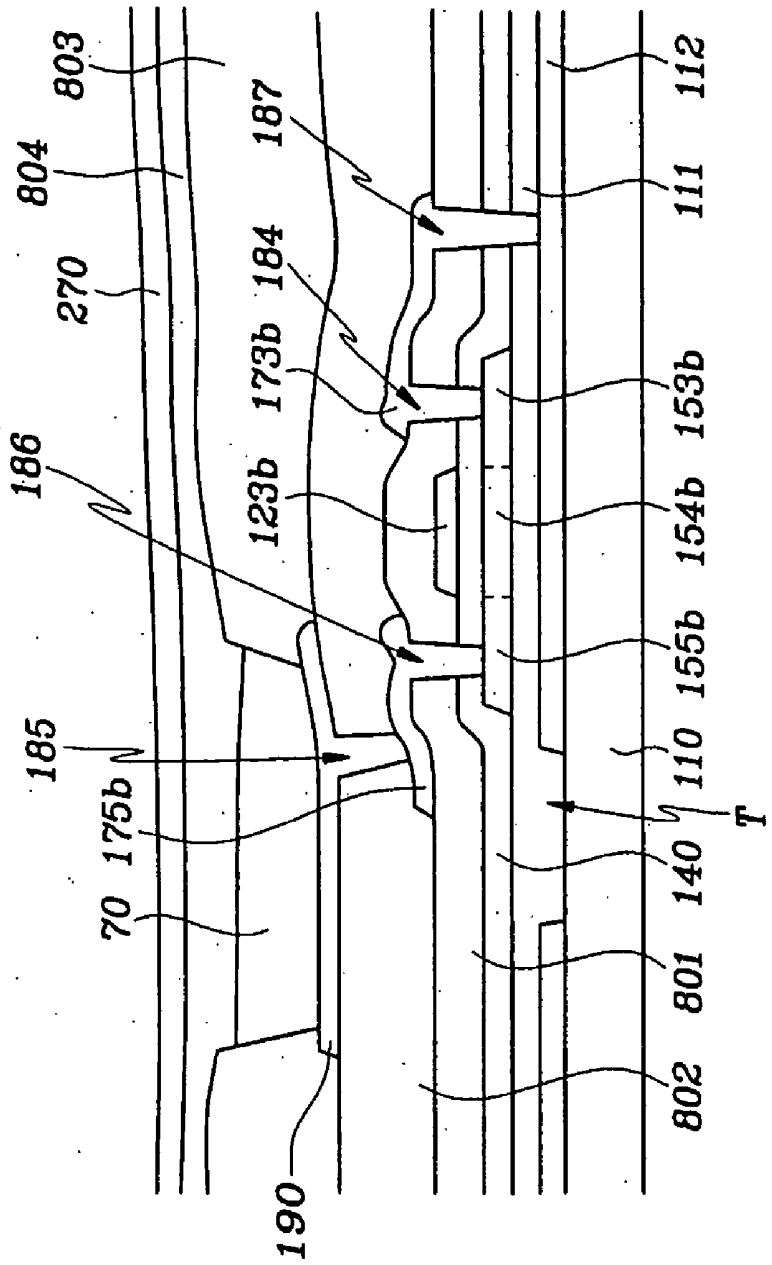
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FIG.14

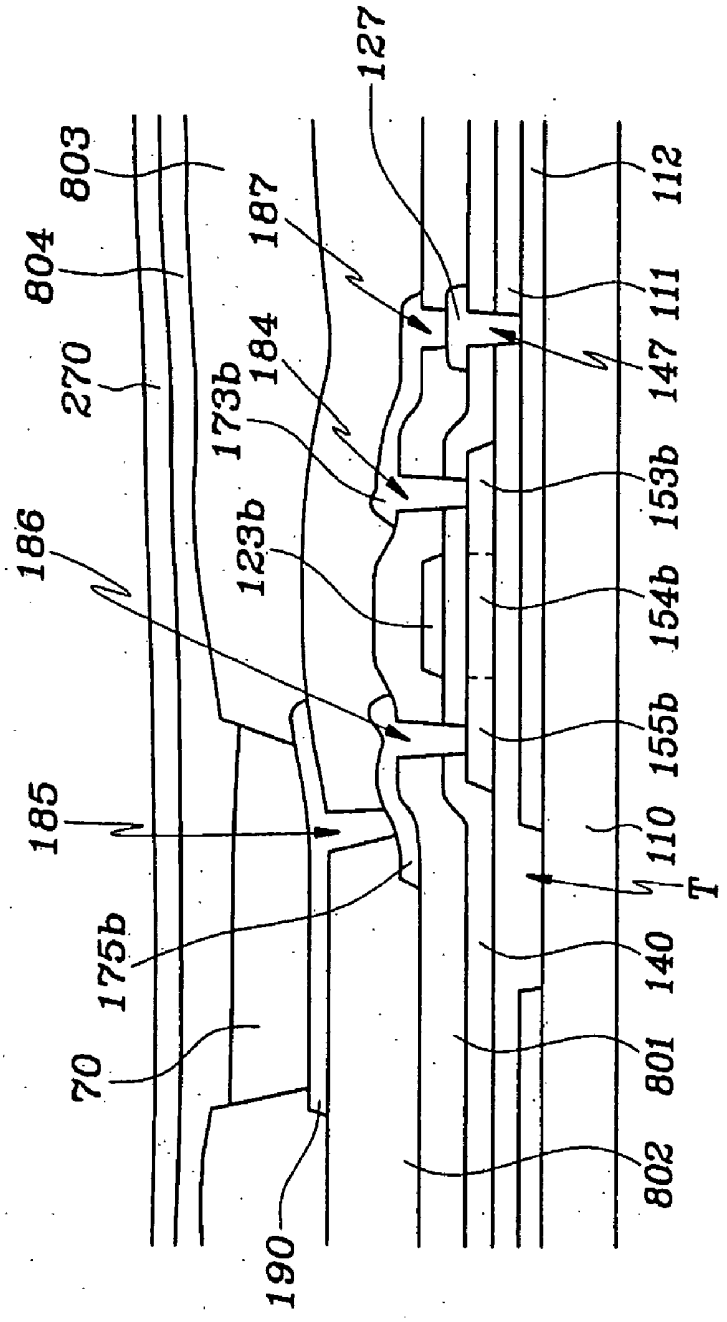
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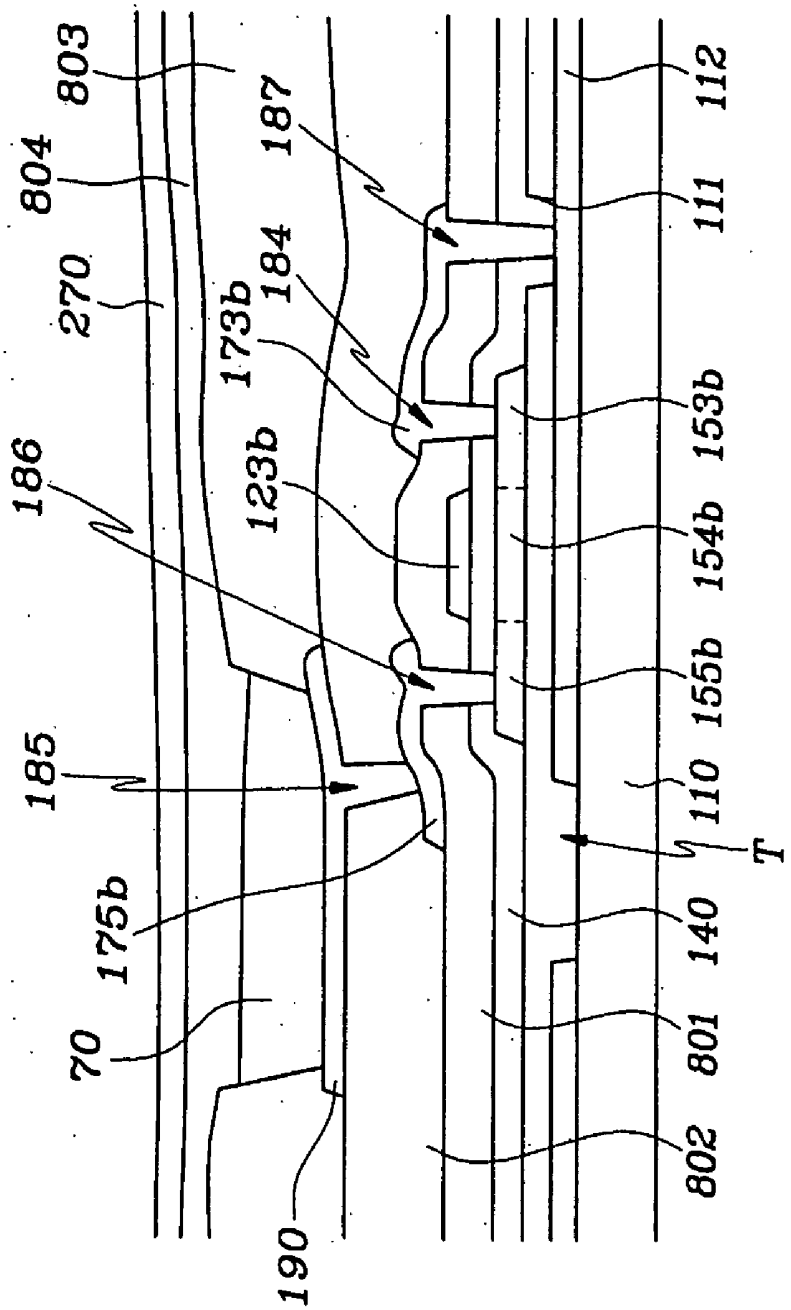
FIG.15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ORGANIC ELECTROLUMINESCENCE DISPLAY PANEL

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to an organic electroluminescence display panel.

[0003] (b) Description of the Related Art

[0004] Generally, an organic electro-luminescence (EL) display is a self emissive display device, which displays images by exciting an emissive organic material to emit light. The organic EL display includes an anode (hole injection electrode), a cathode (electron injection electrode), and an organic light emission layer interposed therebetween. When the holes and the electrons are injected into the light emission layer, they are recombined and pair annihilated with emitting light. The light emission layer further includes an electron transport layer (ETL) and a hole transport layer (HTL) as well as an electron injecting layer (EIL) and a hole injecting layer (HIL) for enhancing the light emission.

[0005] A plurality of pixels of the organic EL display, each including an anode, a cathode, and a light emission layer, are arranged in a matrix and driven in passive matrix (or simple matrix) addressing or active matrix addressing.

[0006] The passive matrix type organic EL display includes a plurality of anode lines, a plurality of cathode lines intersecting the anode lines, and a plurality of pixels, each including a light emission layer. The selection of one of the anode lines and one of the cathode lines cause light emission of a pixel located at the intersection of the selected signal lines.

[0007] The active matrix type organic EL display includes a plurality of pixels, each including a switching transistor, a driving transistor, and a storage capacitor as well as an anode, a cathode, and a light emission layer. The EL display further includes a plurality of gate lines transmitting gate signals and a plurality of data lines transmitting data voltages. The switching transistor is connected to one of the gate lines and one of the data lines and transmits the data voltage from the data line in response to the gate signal. The driving transistor receives the data voltage from the switching transistor and drives a current having a magnitude determined depending on the difference between the data voltage and a predetermined voltage such as a supply voltage. The current from the driving transistor enters the light emission layer to cause light emission having an intensity depending on the current. The storage capacitor is connected between the data voltage and the supply voltage to maintain their voltage difference. The gray scaling of the active matrix type EL display is accomplished by controlling the data voltages to adjust the current driven by the driving transistor. The color representation of the EL display is obtained by providing red, green and blue light emission layers.

[0008] In the meantime, the decrease of the supply voltage reduces the current driven by the driving transistors such that the displayed image is darker than is expected. For example, the data voltages with higher magnitude for displaying higher grays experience higher voltage drop such that the reduction of the currents driven by the driving transistors is much severer. The smaller currents makes the pixels associated therewith emit darker lights, thereby generating cross-talk, which becomes severer as the number of the pixels expected to emit bright lights is increased.

SUMMARY OF THE INVENTION

[0009] A motivation of the present invention is to solve the above-described problems.

[0010] According to an aspect of the present invention, an organic electro-luminescence display panel is provided, which includes: an insulating substrate; a polysilicon layer formed on the substrate; a first insulating layer formed on the polysilicon layer; a gate wire formed on the first insulating layer; a second insulating layer formed on the gate wire; a data wire formed on the second insulating layer and including first and second portions; a pixel electrode connected to the first portion of the data wire; a partition defining an area on the pixel electrode; an organic light emitting member formed in the area on the pixel electrode; a common electrode formed on the light emitting member; and a planar supply voltage electrode disposed between the pixel electrode and the substrate and connected to the second portion of the data wire.

[0011] The supply voltage electrode may be disposed directly on the substrate.

[0012] The organic electro-luminescence display panel may further include a blocking layer formed on the substrate. The blocking layer may have an opening exposing a portion of the supply voltage electrode, the first and the second insulating layers may have a contact hole exposing the exposed portion of the supply voltage electrode through the opening, and the second portion of the data wire may be connected to the supply voltage electrode through the opening and the contact hole. The opening may be larger than the contact hole.

[0013] The polysilicon layer may include first and second transistor portions, each including a channel region, a source region, and a drain region, the gate wire may include first and second gate electrodes overlapping the first and the second transistor portions, respectively, and the data wire may include a first source electrode connected to the source region of the first transistor portion, a first drain electrode connected to the drain region the first transistor portion and the second gate electrode, a second source electrode connected to the source region of the second transistor portion and the supply voltage electrode, and a second drain electrode connected to the drain region of the second transistor portion and the pixel electrode.

[0014] The polysilicon layer may further include a storage electrode region connected to the source region of the second transistor portion and the gate wire further comprises a storage electrode overlapping the storage electrode region and connected to the second gate electrode.

[0015] The pixel electrode may be formed of the same layer or the same material as the data wire.

[0016] The organic electro-luminescence display panel may further include an auxiliary electrode connected between the supply voltage electrode and the second source electrode. The auxiliary electrode may include the same layer as the gate wire.

[0017] The partition preferably includes black photoresist.

[0018] The pixel electrode may be opaque and the common electrode may be transparent. Alternatively, the pixel electrode is transparent and the common electrode is opaque.

[0019] When the pixel electrode is transparent, the supply voltage electrode preferably has a transmitting portion facing the light emitting member for transmitting light from the light emitting member.

[0020] The supply voltage electrode preferably has an opening facing at least a portion of the polysilicon layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:

[0022] **FIG. 1** is a layout view of an organic EL display panel according to an embodiment of the present invention;

[0023] **FIG. 2** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line II-II';

[0024] **FIG. 3** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line III-III';

[0025] **FIG. 4A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a first step of a manufacturing method thereof according to an embodiment of the present invention;

[0026] **FIGS. 4B and 4C** are sectional views of the organic EL display panel shown in **FIG. 4A** taken along the lines IVB-IVB' and IVC-IVC', respectively;

[0027] **FIG. 5A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 4A-4C**;

[0028] **FIGS. 5B and 5C** sectional views of the organic EL display panel shown in **FIG. 5A** taken along the lines VB-VB' and VC-VC', respectively;

[0029] **FIG. 6A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 5A-5C**;

[0030] **FIGS. 6B and 6C** are sectional views of the organic EL display panel shown in **FIG. 6A** taken along the lines VIB-VIB' and VIC-VIC', respectively;

[0031] **FIG. 7A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 6A-6C**;

[0032] **FIGS. 7B and 7C** are sectional views of the organic EL display panel shown in **FIG. 7A** taken along the lines VIIB-VIIB' and VIIC-VIIC', respectively;

[0033] **FIG. 8A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 7A-7C**;

[0034] **FIGS. 8B and 8C** sectional views of the organic EL display panel shown in **FIG. 8A** taken along the lines VIIIB-VIIIB' and VIIIC-VIIIC', respectively;

[0035] **FIG. 9A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 8A-8C**;

[0036] **FIGS. 9B and 9C** are sectional views of the organic EL display panel shown in **FIG. 9A** taken along the lines IXB-IXB' and IXC-IXC', respectively;

[0037] **FIG. 10A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 9A-9C**;

[0038] **FIGS. 10B and 10C** are sectional views of the organic EL display panel shown in **FIG. 10A** taken along the lines XB-XB' and XC-XC', respectively;

[0039] **FIG. 11** is a layout view of a bottom emission type organic EL display panel according to an embodiment of the present invention;

[0040] **FIG. 12** is an exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XII-XII';

[0041] **FIG. 13** is an exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XIII-XIII';

[0042] **FIG. 14** is another exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XIII-XIII'; and

[0043] **FIG. 15** is another exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XIII-XIII'.

DETAILED DESCRIPTION OF EMBODIMENTS

[0044] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[0045] In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region, substrate or panel is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0046] Then, organic electroluminescence display devices and manufacturing methods thereof according to embodiments of the present invention will be described with reference to the accompanying drawings.

[0047] First, an organic EL display according to an embodiment of the present invention is described in detail with reference to **FIGS. 1-3**.

[0048] **FIG. 1** is a layout view of an organic EL display panel according to an embodiment of the present invention, **FIG. 2** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line II-II', and **FIG. 3** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line III-III'.

[0049] A supply voltage electrode **112** supplied with a predetermined voltage such as a supply voltage is formed on an insulating substrate **10** preferably made of transparent glass or silicon wafer. The supply voltage electrode **112** is

preferably made of a conductive material having low resistivity such as Al, Al alloy, Ag, or Ag alloy and it substantially covers an entire surface of the substrate **110** to have a planar shape without having a stripe shape.

[**0050**] A blocking layer **111** preferably made of silicon oxide or silicon nitride is formed on the supply voltage electrode **112**.

[**0051**] A polysilicon layer including a plurality of pairs of a first transistor portion **150***a* for a switching thin film transistor (TFT) and a second transistor portion **150***b* for a driving TFT is formed on the blocking layer **111**.

[**0052**] The first transistor portion **150***a* includes a plurality of impurity regions such as a (first) source region **153***a*, an intermediate region **152***a*, and a (first) drain region **155***a*, which are doped with n type impurity and separated from one another, and a plurality of intrinsic regions such as a pair of (first) channel regions **154***a* disposed between the impurity regions **153***a*, **152***a* and **155***a*. The first source region **153***a* extends to form a storage electrode region **157**.

[**0053**] The second transistor portion **150***b* includes a plurality of impurity regions such as a (second) source region **153***b* and a (second) drain region **155***b*, which are doped with p type impurity, and an intrinsic region such as a (second) channel region **154***b* disposed between the impurity regions **153***b* and **155***b*.

[**0054**] Alternatively, the impurity regions **153***a*, **152***a* and **155***a* of the first transistor portion **150***a* are doped with p type impurity, while the impurity regions **153***b* and **155***b* of the second transistor portion **150***b* are doped with n type impurity, depending on driving conditions.

[**0055**] A gate insulating layer **140** preferably made of silicon oxide or silicon nitride is formed on the polysilicon layer **150***a* and **150***b*.

[**0056**] A plurality of gate lines **121** including a plurality of pairs of first gate electrodes **123***a* and a plurality of second gate electrodes **123***b*, which are preferably made of low resistivity material such as Al or Al alloy, are formed on the gate insulating layer **140**. Each pair of first gate electrodes **123***a* are branched from the gate line **121** and they intersect the first transistor portion **150***a* such that they overlap the pair of the first channel regions **154***a*. Each second gate electrode **123***b* is separated from the gate line **121** and it intersects the second transistor portion **150***b* such that it overlaps the second channel region **154***b*. The second gate electrode **123***b* extends to form a storage electrode **133** overlapping the storage electrode region **157** of the polysilicon layer **150***a* and **150***b* to form a storage capacitor.

[**0057**] A first interlayer insulating film **801** is formed on the gate lines **121** and the first and the second gate electrodes **123***a* and **123***b*.

[**0058**] A plurality of data lines **171**, each including a plurality of first source electrodes **173***a*, a plurality of second source electrodes **173***b*, and a plurality of first and second drain electrodes **175***a* and **175***b* are formed on the first interlayer insulating film **801**.

[**0059**] Each first source electrode **173***a* is branched from the data line **171** and connected to the first source region **153***a* through a contact hole **181** penetrating the first interlayer insulating film **801** and the gate insulating layer **140**. Each first drain electrode **175***a* is connected to the first drain region **155***a* through a contact hole **182** penetrating the first interlayer insulating film **801** and the gate insulating layer **140**. The first drain electrode **175***a* is also connected to the second gate electrode **123***b* through a contact hole **183** penetrating the first interlayer insulating film **801** and the gate insulating layer **140**.

[**0060**] Each second source electrode **173***b* has an island shape and it is connected to the second source region **153***b* through a contact hole **184** penetrating the first interlayer insulating film **801** and the gate insulating layer **140**. Each second drain electrode **175***b* is connected to the second drain region **155***b* through a contact hole **186** penetrating the first interlayer insulating film **801** and the gate insulating layer **140**. The second source electrode **173***b* is also connected to the supply voltage electrode **112** through a contact hole **187** penetrating the first interlayer insulating film **801**, the gate insulating layer **140**, and the blocking layer **111**.

[**0061**] A second interlayer insulating film **802** is formed on the data lines **171**, the source electrodes **173***a* and **173***b*, and the drain electrodes **175***a* and **175***b*. The second interlayer insulating film **802** is preferably made of silicon nitride, silicon oxide, or organic insulating material and it has a plurality of contact holes **185** exposing the second drain electrodes **175***b*.

[**0062**] A plurality of pixel electrodes **190** are formed on the second interlayer insulating film **802**. Each pixel electrode **190** is connected to the second drain electrode **175***b* through the contact hole **185** and it is preferably made of reflective opaque material such as Al or Ag alloy. However, the pixel electrode **190** may be formed of a transparent conductive material such as ITO (indium tin oxide) and IZO (indium zinc oxide). The pixel electrode **190** may be incorporated with the second drain electrode **175***b* for reducing the manufacturing cost.

[**0063**] A partition **803** for separating pixels of the organic EL display panel is formed on the second interlayer insulating film **802** and the pixel electrodes **190**. The partition **803** surrounds the pixel electrodes **190** like a bank to define depressions filled with organic light emitting material. The partition **803** is preferably made of organic insulating material and, more preferably, made of a photosensitive material containing black pigment, which is exposed to light and developed, such that the partition **803** functions as a light blocking member and a manufacturing method thereof is simplified.

[**0064**] A plurality of light emitting members **70** are formed on the pixel electrodes **190** and disposed in the depressions defined by the partition **803**. The light emitting members **70** are preferably made of organic material emitting primary-color lights such as red, green and blue lights. The red, green and blue light emitting members **70** are arranged periodically.

[**0065**] A buffer layer **804** is formed on the light emitting members **70** and the partition **803**. The buffer layer **804** may be omitted if it is not required.

[**0066**] A common electrode **270** supplied with a predetermined voltage is formed on the buffer layer **804**. The common electrode **270** is preferably made of transparent conductive material such as ITO and IZO. If the pixel

electrodes **190** are transparent, the common electrode **270** is preferably made of reflective opaque metal such as Al.

[**0067**] An auxiliary electrode (not shown) made of low resistivity material is optionally provided for compensating the conductivity of the common electrode **270**. The auxiliary electrode may be disposed between the common electrode **270** and the buffer layer **804** or on the common electrode **270**, and it preferably has a matrix form and is disposed along the partition **803** such that it does not overlap the light emitting member **70**.

[**0068**] In the above-described organic EL display panel, the first transistor portion **150***a*, the first gate electrode **123***a* connected to the gate line **121**, the first source electrode **153***a* connected to the data line **171**, and the first drain electrode **155***a* form a switching TFT. In addition, the second transistor portion **150***b*, the second gate electrode **123***b* connected to the first drain electrode **155***a*, the second source electrode **153***b* connected to the supply voltage electrode **112**, and the second drain electrode **155***b* connected to the pixel electrode **190** form a driving TFT. Furthermore, the pixel electrode **190** and the common electrode **270** serve as an anode and a cathode, respectively, and the storage electrode region **157** connected to the first drain region **155***a* and the storage electrode **133** connected to the supply voltage electrode **112** through the second source electrode **153***b* form a storage capacitor.

[**0069**] The switching TFT transmits the data voltage from the data line **171** to the driving TFT in response to the gate signal from the gate line **121**. Upon the receipt of the data voltage, the driving TFT generates a current having a magnitude depending on the difference between the data voltage and the supply voltage. In addition, the data voltage is charged in the storage capacitor to be maintained after the switching TFT is turned off. The current driven by the driving TFT enters into the light emitting member **70** through the pixel electrode **190** and reaches the common electrode **270**. The current flowing in the light emitting member **70** means that positive charge carriers such as holes and negative charge carriers such as electrons are injected into the light emitting member **70** from the anode **190** and the cathode **270**, respectively, and they are drifted by an electric field generated by the voltage difference between the anode **190** and the cathode **270**. The holes and the electrons in the light emitting member **70** then meet each other to be recombined into excitons, which emit light with a predetermined wavelength. The intensity of the emitted light depends on the current driven by the driving TFT and flowing in the light emitting member **70**.

[**0070**] The emitted light goes out of the display panel after passing through the common electrode **270** or the pixel electrode **190**. A transparent common electrode **270** and an opaque pixel electrode **190** are applicable to a top emission type EL display, which displays an image on its top surface. On the contrary, a transparent pixel electrode **190** and an opaque common electrode **270** are applicable to a bottom emission type EL display, which displays an image on its bottom surface. In the former case, the supply voltage electrode **112** can have various positions or arrangements between the light emitting members **70** and the substrate **111**. In the latter case, the supply voltage electrode **112** may be transparent at least in part in order to transmit the light emitted from the light emitting members **70**.

[**0071**] As described above, since the supply voltage electrode **112** has a planar shape covering the entire surface of the organic EL display panel, the magnitude of the supply voltage applied to the pixels is almost constant. In addition, since the supply voltage electrode **112** has a sheet resistance, a voltage drop may not significantly differentiate the magnitude of the supply voltage applied to the pixels. Therefore, a cross-talk resulted from the difference in the brightness between the pixels is significantly reduced.

[**0072**] Now, a method of manufacturing the organic EL display panel shown in **FIGS. 1-3** is described with reference to **FIGS. 4A-10C** as well as **FIGS. 1-3**.

[**0073**] **FIGS. 4A, 5A**, 6A, 7A, 8A, 9A and **10**A are layout views of the organic EL display panel shown in **FIGS. 1-3** in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, **FIGS. 4B, 5B**, 6B, 7B, 8B, 9B and **10**B are sectional views of the organic EL display panels shown in **FIGS. 4A, 5A**, 6A, 7A, 8A, 9A and **10**A taken along the lines IVB-IVB', VB-VB', VIB-VIB', VIIB-VIIB', VIIIB-VIIIB', IXB-IXB', and XB-XB', respectively, and **FIGS. 4C, 5C**, 6C, 7C, 8C, 9C and **10**C are sectional views of the organic EL display panels shown in FIGS. **4**A, **5**A, **6**A, **7**A, **8**A, **9**A and **10**A taken along the lines IVC-IVC', VB-VC', VIC-VIC', VIIC-VIIC', VIIIC-VIIIC', IXC-IXC', and XC-XC', respectively.

[**0074**] Referring to **FIGS. 4A-4C**, a conductive material is deposited on an insulating substrate **110** to form a supply voltage electrode **112**. The supply voltage electrode **112** may be photo-etched to form openings or transmitting portions therein.

[**0075**] A blocking layer **111** preferably made of silicon oxide is formed on an insulating substrate **110**, and an amorphous silicon layer is deposited on the blocking layer **111**. The deposition of the amorphous silicon layer is preferably performed by LPCVD (low temperature chemical vapor deposition), PECVD (plasma enhanced chemical vapor deposition) or sputtering. Consecutively, the amorphous silicon layer is laser-annealed to be crystallized into a polysilicon layer.

[**0076**] Next, the polysilicon layer is photo-etched to form a plurality of pairs of first and second transistor portions **150***a* and **150***b*.

[**0077**] Referring to **FIGS. 5A-5C**, a gate insulating layer **140** is deposited on the polysilicon layer **150***a* and **150***b*.

[**0078**] Successively, a gate metal layer is deposited on the gate insulating layer **140** and a photoresist film is coated, exposed to light, and developed to form a first photoresist PR1. The gate metal layer is etched by using the first photoresist PR1 as an etch mask to form a plurality of gate electrodes **123***b* including storage electrodes **133** and a plurality of gate metal members **120**. P type impurity is injected into exposed portions of the second transistor portions **150***b* of the polysilicon layer to form a plurality of P type impurity regions **153***b* and **155***b*. At this time, the first transistor portions **150***a* of the polysilicon layer are covered with the first photoresist PR1 and the gate metal members **120** to be protected from impurity implantation.

[**0079**] Referring to **FIGS. 6A-6C**, the first photoresist PR1 is removed and another photoresist film is coated, exposed to light, and developed to form a second photoresist

PR2. The gate metal layer **120** is etched by using the first photoresist PR2 as an etch mask to form a plurality of gate lines **121** including gate electrodes **123***a*. N type impurity is injected into exposed portions of the first transistor portions **150***a* of the polysilicon layer to form a plurality of N type impurity regions **153***a* and **155***a*. At this time, the second transistor portions **150***b* of the polysilicon layer are covered with the second photoresist PR2 to be protected from impurity implantation.

[**0080**] Referring to **FIGS. 7A-7C**, a first interlayer insulating film **801** is deposited on the gate lines **121** and the gate electrodes **123***a* and **123***b*. The first interlayer insulating film **801**, the gate insulating layer **140**, and the blocking layer **111** are photo-etched form a plurality of contact holes **181**, **182**, **184** and **186** exposing the impurity regions **153***a*, **155***a*, **153***b* and **155***b*, respectively, as well as a plurality of contact holes **183** and **187** exposing the gate electrodes **123***b* and portions of the supply voltage electrode **112**.

[**0081**] Referring to **FIGS. 8A-8C**, a data metal layer is deposited and photo-etched to form a plurality of data lines **171** including first source electrodes **173***a*, a plurality of second source electrodes **173***b*, a plurality of first and second drain electrodes **175***a* and **175***b*.

[**0082**] Referring to **FIGS. 9A-9C**, a second interlayer insulating film **802** is deposited on the data lines **171**, the source electrodes **173***a* and **173***b*, and the drain electrodes **175***a* and **175***b* as well as on the first interlayer insulating film **801**. The second interlayer insulating film **802** is photo-etched to form a plurality of contact holes **185** exposing the second drain electrodes **175***b*.

[**0083**] Referring to **FIGS. 10A-10C**, a transparent conductive material or a low resistivity reflective material is deposited and patterned to form a plurality of pixel electrodes **190**. When the pixel electrodes **190** are made of reflective opaque material, they may be formed of the data metal layer along with the data lines **171**.

[**0084**] Referring to **FIGS. 1-3**, an organic film containing black pigment is coated on the pixel electrodes **190** and the second interlayer insulating film **802**, and it is exposed to light and developed to form a partition **803** defining a plurality of depressions on the pixel electrodes **190**. Thereafter, a plurality of organic light emitting members **70** are formed in the depressions by deposition or inkjet printing following a masking. The organic light emitting member **70** preferably has a multi-layered structure.

[**0085**] Next, an organic conductive material is deposited on the light emitting members **70** to form a buffer layer **804**, and ITO or IZO is deposited on the buffer layer **804** to form a common electrode **270**.

[**0086**] An auxiliary electrode (not shown) made of low resistivity material such as Al may be formed before or after the formation of the common electrode **270**.

[**0087**] As described above, a top emission type organic EL display panel according to this embodiment includes an opaque pixel electrode and a transparent common electrode **270**, and it displays an image on its top surface. The supply voltage electrode **112** can be placed on another position under the organic light emitting member **70**.

[**0088**] Next, a bottom emission type organic EL display panel including a transparent pixel electrode and an opaque common electrode for displaying an image on its bottom surface is described in detail with reference to **FIGS. 11-15**.

[**0089**] **FIG. 11** is a layout view of a bottom emission type organic EL display panel according to an embodiment of the present invention and **FIGS. 12 and 13** are exemplary sectional views of the display panel shown in **FIG. 11** taken along the lines XII-XII' and XIII-XIII', respectively.

[**0090**] As shown in **FIGS. 11-13**, a structure of an organic EL display panel according to this embodiment is similar to that shown in **FIGS. 1-3**.

[**0091**] In detail, a supply voltage electrode **112** and a blocking layer **111** are sequentially formed on an insulating substrate **110**. A polysilicon layer including a plurality of pairs of a first transistor portion **150***a* for a switching TFT and a second transistor portion **150***b* for a driving TFT is formed on the blocking layer **111**, and a gate insulating layer **140** is formed thereon. The first transistor portion **150***a* includes a plurality of impurity regions such as a first source region **153***a*, an intermediate region **152***a*, and a first drain region **155***a*, and a pair of first channel regions **154***a* disposed between the impurity regions **153***a*, **152***a* and **155***a*. The second portion **150***b* includes a second source region **153***b*, a second drain region **155***b*, and a second channel region **154***a* disposed between the second source region **153***b* and the second drain region **155***a*. A plurality of gate lines **121** including first gate electrodes **123***a* and a plurality of second gate electrodes **123***b* including storage electrodes **133** are formed on the gate insulating layer **140**, and a first interlayer insulating film **801** is formed thereon. A plurality of data lines **171** including first source electrodes **173***a*, a plurality of second source electrodes **173***b*, and a plurality of first and second drain electrodes **175***a* and **175***b* are formed on the first interlayer insulating film **801**, and a second interlayer insulating film **802** is formed thereon. A plurality of pixel electrode **190** and a partition **803** defining a plurality of depressions on the pixel electrodes **190** are formed on the second interlayer insulating film **802**, and a plurality of organic light emitting member **70** are formed in the depressions on the pixel electrodes **190**. A buffer layer **804** is formed on the organic light emitting members **70** and the partition **803**, and a common electrode **270** is formed on the buffer layer **804**.

[**0092**] The pixel electrodes **190** are transparent while the common electrode **270** is opaque. The supply voltage electrode **112** has a plurality of transmitting portions T facing the pixel electrodes **190** for the transmission of light emitted from the light emitting members **70**. In addition, the supply voltage electrode **112** has a plurality of openings S facing the channel regions **154***a* of the first transistor portions **150***a* for minimizing the effect of a supply voltage on the switching TFTs.

[**0093**] A manufacturing method of the organic EL display panel shown in **FIGS. 11-13** according to an embodiment of the present invention forms the openings S and the transmitting portions T by patterning the supply voltage electrode **112** using a photolithography process after depositing the supply voltage electrode **112**.

[**0094**] The area of the transmitting portions T of the planar supply voltage electrode **112** according to this embodiment can be increased compared with a conventional linear supply voltage electrode.

[0095] **FIG. 14** is another exemplary sectional view of the display panel shown in **FIG. 11** taken along the lines XIII-XIII'.

[0096] Referring to **FIG. 14**, a plurality of auxiliary members **127** for compensating the connection between the supply voltage electrode **112** and the second source electrodes **173***b* are formed on the gate insulating layer **140**. The auxiliary members **127** are connected to the supply voltage electrode **112** through contact holes **147** penetrating the gate insulating layer **140** and the blocking layer **111**, and also connected to the second source electrodes **173***b* through contact holes **187** penetrating the first interlayer insulating film **801**. The auxiliary members **127** are preferably made of the same layer as the gate lines **121**.

[0097] **FIG. 15** is another exemplary sectional view of the display panel shown in **FIG. 11** taken along the lines XIII-XIII'.

[0098] Referring to **FIG. 15**, the blocking layer **111** has a plurality of openings **117** exposing the supply voltage electrode **112** and a plurality of contact holes **187** penetrating the first interlayer insulating film **801** and the gate insulating layer **140** and having smaller size than the openings **117** are formed in the openings **117**. The second source electrodes **173***b* are connected to the supply voltage electrodes **112** through the contact holes **187**.

[0099] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

1-16. (canceled)

17. An organic electro-luminescence display (OELD), comprising:

a substrate;

a conductive layer formed on the substrate;

an insulating layer formed on the conductive layer;

a gate wire formed on the insulating layer;

a data wire formed on the insulating layer and insulated from the gate wire and electrically connected to the conductive layer;

a pixel electrode connected to the data wire;

an organic light emitting member formed on the pixel electrode; and

a common electrode formed on the organic light emitting member.

18. The OELD of claim 17, further comprising a thin film transistor (TFT) having a gate electrode, a source electrode and a drain electrode, wherein the source electrode is connected to the data wire.

19. The OELD of claim 18, further comprising an auxiliary member electrically connecting the conductive layer and the data wire.

20. The OELD of claim 17, wherein a supply voltage is applied to the conductive layer.

21. The OELD of claim 17, wherein the pixel electrode is formed of an opaque material.

22. The OELD of claim 17, wherein the pixel electrode is formed of a transparent conductive material.

23. The OELD of claim 22, wherein the conductive layer has a transmitting window corresponding to the pixel electrode.

24. The OELD of claim 18, wherein the conductive layer has an opening overlapping at least a portion of the TFT.

25. The OELD of claim 17, further comprising a partition surrounding the organic light emitting member.

26. The OELD of claim 25, wherein the partition is form of a photosensitive material containing black pigments.

27. An organic electro-luminescence display (OELD), comprising:

a substrate;

a conductive layer formed on the substrate and receiving a supply voltage;

an insulating layer formed on the conductive layer;

a first thin film transistor (TFT) formed on the insulating layer;

a pixel electrode connected to the first TFT;

an organic light emitting member formed on the pixel electrode; and

a common electrode formed on the organic light emitting member.

28. The OELD of claim 27, further comprising;

a second TFT formed on the insulating layer and connected with the pixel electrode;

a gate wire formed on the first insulating layer; and

a data wire formed on the insulating layer and insulated from the gate wire.

29. The OELD of claim 28, wherein a portion of the data wire is connected to the conductive layer.

30. The OELD of claim 28, wherein the first TFT has a first gate electrode, a first source electrode, and a first drain electrode, and the second TFT has a second gate electrode, a second source electrode, and a second drain electrode, and

the first gate electrode is connected to the gate wire, the first source electrode is connected to the data wire, the first drain electrode is connected to the second gate electrode, the second source electrode is connected to the data wire, and the second drain electrode is connected to the pixel electrode.

31. The OELD of claim 30, further comprising an auxiliary member electrically connecting the conductive layer and the second TFT.

32. The OELD of claim 27, wherein the pixel electrode is made of an opaque metal.

33. The OELD of claim 27, wherein the pixel electrode is made of a transparent conductive material.

34. The OELD of claim 33, wherein the conductive layer has a transmitting window corresponding to the pixel electrode.

35. The OELD of claim 27, wherein the conductive layer has an opening overlapping at least a portion of the first TFT.

36. The OELD of claim 28, wherein the conductive layer has a first opening overlapping at least a portion of the first TFT and a second opening overlapping at least a portion of the second TFT.

* * * * *

专利名称(译)	有机电致发光显示板		
公开(公告)号	US20050280039A1	公开(公告)日	2005-12-22
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[标]申请(专利权)人(译)	CHOI BEOHM ROCK 柴CHONG CHUL SHIN KYONG JU		
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IPC分类号	H01L51/50 G09F9/30 G09G3/30 H01J1/62 H01L21/77 H01L27/10 H01L27/12 H01L27/32 H01L31/109 H05B33/02 H05B33/12 H05B33/14 H05B33/26		
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摘要(译)

根据本发明的一个方面，提供了一种有机电致发光显示板，包括：绝缘基板;形成在基板上的多晶硅层;形成在多晶硅层上的第一绝缘层;栅极线形成在第一绝缘层上;形成在栅极线上的第二绝缘层;数据线形成在第二绝缘层上并包括第一和第二部分;像素电极连接到数据线的第一部分;限定像素电极上的区域的分区;有机发光构件形成在像素电极上的区域中;形成在发光元件上的公共电极;平面电源电压电极，设置在像素电极和基板之间，并连接到数据线的第二部分。